EE 505

Lecture 3

Data Converter Operation and Characterization

-- Linearity Metrics

REVIEW

Integral Nonlinearity (DAC)

Nonideal DAC



REVIEW

Integral Nonlinearity (ADC)

Continuous-input based INL definition



REVIEW

Integral Nonlinearity (ADC)

Nonideal ADC





Place N-3 uniformly spaced points between X_{T1} and X_{T(N-1)} designated \mathcal{X}_{FTk} INL_k= \mathcal{X}_{Tk} - \mathcal{X}_{FTl} 1 ≤ k ≤ N-2 INL = $\max_{2 \le k \le N-2} \{|NL_k|\}$

Characteristics Dominantly Depend Upon Random Variables

- Static characteristics
 - Resolution
 - Least Significant Bit (LSB)
 - Offset and Gain Errors
 - Absolute Accuracy
 - Relative Accuracy
 - Integral Nonlinearity (INL)
 - Differential Nonlinearity (DNL)
 - Monotonicity (DAC)
 - Missing Codes (ADC)
 - Quantization Noise
 - Low-f Spurious Free Dynamic Range (SFDR)
 - Low-f Total Harmonic Distortion (THD)
 - Effective Number of Bits (ENOB)
 - Power Dissipation

Characteristics Dominantly Depend Upon Random Variables

- Dynamic characteristics
 - Conversion Time or Conversion Rate (ADC)
 - Settling time or Clock Rate (DAC)
 - Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
 - Dynamic Range
 - Spurious Free Dynamic Range (SFDR)
 - Total Harmonic Distortion (THD)
 - Signal to Noise Ratio (SNR)
 - Signal to Noise and Distortion Ratio (SNDR)
 - Sparkle Characteristics
 - Effective Number of Bits (ENOB)

Methods of Characterizing how Random Variables Affect Performance

- Analytical Statistical Formulation and Analysis
- MATLAB Simulations (often using Monte-Carlo Analysis)
- Spectre/Spice Monte-Carlo Simulations
- Ignore Effects of Random Effects

How important is statistical characterization of data converters?

Example: 7-bit FLASH ADC with R-string DAC

Assume R-string is ideal, V_{REF} =1V and V_{OS} for each comparator must be at most +/- $\frac{1}{2}$ LSB

Why this assumption?

Case 1

Determine the yield if V_{OS} has a Gaussian distribution (Normal) with zero mean and a standard deviation of 5mV



Example: 7-bit FLASH ADC with R-string DAC

Assume R-string is ideal, V_{REF} =1V and V_{OS} for each comparator must be at most +/- $\frac{1}{2}$ LSB



Case 1

Determine the yield if $V_{\text{OS}}\,$ has a Gaussian distribution (Normal) with zero mean and a standard deviation of 5mV

1/2 LSB = 1V/(2⁽⁷⁺¹⁾)=3.9mV

The probability that a single comparator meets the V_{OS} requirement is given by





 $P_{COMP} = 2 \bullet F_N(0.78) - 1 = 2 \bullet .7823 - 1 = 0.565$

Each comparator has 56.5% yield

Example: 7-bit FLASH ADC with R-string DAC

Case 1 σ_{VOS} =5mV

 $P_{COMP} = 0.565$

Since all comparators must be good, the ADC yield is

$$Y_{ADC} = (P_{COMP})^{127} = (0.565)^{127}$$

 $Y_{ADC} = 3.2 \bullet 10^{-32}$

This yield is essentially 0 and a standard deviation of 5mV is even not trivial to obtain with MOS comparators !

The effects of statistical variation can have dramatic effects on yield of data converters !



An ideal ADC has a monotone relationship between analog inputs and digital output

If expressed in thermometer code, the "thermometer" output never decreases with increasing inputs

Occasionally, some ADCs will exhibit one or more outputs where the Boolean output drops rather than increases

This flash structure naturally provides a thermometer code output. If the thermometer code output is not monotone, we say it has a bubble Major errors can occur in the TBD if a bubble exists in the thermometer code output



Occasionally, some ADCs will have one or more outputs that <u>appear</u> to be almost unrelated to the input (very large error in output, maybe only for small range of outputs or maybe only occur once in a while)

If this happens, the data converter is said to have "Sparkle"

This ADC architecture is vulnerable to sparkle if bubbles exist in the thermometer output code and the TBD, a logic circuit, does not appropriately handle them

Example: 7-bit FLASH ADC with R-string DAC

Case 1 σ_{VOS} =5mV

Since all comparators must be good, the ADC yield is

 $Y_{ADC} = 3.2 \bullet 10^{-32}$



Note: The specification in this example that requires no comparator has an offset voltage of larger than 0.5LSB may not be a good performance specification as the FLASH ADC may actually perform reasonably well even if some comparators have an offset that is larger than 0.5LSB. A more useful requirement might be that there be no bubbles in the thermometer code output. Certainly if all comparators have an offset that is at most 0.5LSB, there will be no bubbles in the output code attributable to comparator offset but a modestly weaker constraint can also guarantee there are no bubbles. With the 0.5LSB assumption, a specification that was dependent upon 127 uncorrelated random variables was obtained which made the analysis quite easy. A "no bubble" specification could be approximated by stating that the maximum of the 127

Example: 7-bit FLASH ADC with R-string DAC



This modest change in the offset voltage has increased the yield to 98.8%

Example: What will be the yield if two of the 7-bit FLASH ADCs with yields of 98.8% are combined to obtain an 8-bit ADC?



Example: What will be the yield if two of the 7-bit FLASH ADCs with yields of 98.8% are combined to obtain an 8-bit ADC?

Since one additional bit has been added, $V_{\rm LSB}$ will decrease From 7.8mV to 3.9mV. Thus $^{1\!\!/_2}$ LSB will be reduced to 1.95mV

1.95 mV

$$P_{COMP} = \int_{-1.95mV}^{1.95mV} f_{VOS} dV$$
With the same $\sigma_{VOS} = 1mV$, $X_N = 1.95mV/1mV = 1.95$

$$P_{COMP} = \int_{-1.95}^{1.95} f_N dx \qquad P_{COMP} = 2 \cdot F_N (1.95) - 1 = 2 \cdot 0.97441 - 1 = 0.9488$$

$$Y_{ADC} = (P_{COMP})^{255} = (0.9488)^{255}$$

$$Y_{ADC} = 1.52 \cdot 10^{-6}$$

This seemingly simple extension of a circuit with a very high yield has essentially no yield !

- Statistical analysis of data converters is critical
- Some architectures are more sensitive than others to statistical variations in components
- The onset of yield loss due to statistical limitations is generally quite abrupt and can have disastrous effects if not considered as part of the design process

Recall examples where σ_{VOS} =5mV compared with σ_{VOS} =1mV

 Substantially over-designing to avoid concerns about statistical yield loss is not a practical solution since the area penalty, the speed penalty, and the power penalty are generally quite severe

For the effects of local random variations of a parameter X, generally

$$\sigma_X \propto \frac{A_0}{\sqrt{A_C}}$$

where A_C is the area of the matching critical components and A_0 is a process parameter

Importance of statistical analysis – example

What changes in area would be needed to decrease $\sigma_{\text{VOS}}~$ from 5mV to 1mV?



 $A_{C_1} = 25A_{C_5}$

Equivalent Number of Bits (ENOB)

- Often the performance of an n-bit data converter is not commensurate with that of an ideal n-bit data converter but more like that of an n-k bit data converter
- The equivalent number of bits (ENOB) is often used to characterize the actual level of performance
- Different ENOB definitions depending upon which characterization parameter is of interest (e.g. INL, SFDR, SNR, ...)

Consider initially the continuous INL definition for an ADC where the INL of an ideal ADC is $X_{LSB}/2$

Assume INL=
$$vX_{LSBR} = v \frac{X_{REF}}{2^{n_R}}$$

where X_{LSBR} is the LSB based upon the defined resolution , n_{R}

Define the equivalent LSB by

$$X_{LSBE} = \frac{X_{REF}}{2^{n_{EQ}}}$$

Thus (substituting for X_{REF} into INL expression):

INL=
$$v \frac{2^{n_{EQ}}}{2^{n_{R}}} X_{LSBE} = \left[v 2^{n_{EQ}+1-n_{R}}\right] \frac{X_{LSBE}}{2}$$

Since an ideal ADC has an INL of $X_{LSB}/2$, Setting term in [] to 1, can solve for n_{EQ} to obtain

$$ENOB = n_{EQ} = n_{R} - 1 - \log_2(v)$$

where n_R is the defined resolution

Observe: the ENOB based upon the INL has been defined as the maximum deviation from the end-point fit line

INL-based ENOB ENOB = n_R -1-log₂(v)

Consider an ADC with specified resolution of n_R and INL of v LSB

V	ENOB
1/2	n _R
1	n _R -1
2	n _R -2
4	n _R -3
8	n _R -4
16	n _R -5

Though based upon the continuous-INL definition, often used to define ENOB from INL viewpoint



16-Bit, 200 MSPS/250 MSPS Analog-to-Digital Converter

Data Sheet

\$120 in 1000's

AD9467

FEATURES

75.5 dBFS SNR to 210 MHz at 250 MSPS 90 dBFS SFDR to 300 MHz at 250 MSPS SFDR at 170 MHz at 250 MSPS 92 dBFS at -1 dBFS 100 dBFS at -2 dBFS 60 fs rms jitter Excellent linearity at 250 MSPS $DNL = \pm 0.5 LSB typical$ INL = ±3.5 LSB typical 2V p-p to 2.5 V p-p (default) differential full-scale input (programmable) Integrated input buffer External reference support option Clock duty cycle stabilizer Output clock available Serial port control Built-in selectable digital test pattern generation Selectable output data format LVDS outputs (ANSI-644 compatible)

1.8 V and 3.3 V supply operation

APPLICATIONS

Multicarrier, multimode cellular receivers Antenna array positioning Power amplifier linearization Broadband wireless Radar Infrared imaging Communications instrumentation

FUNCTIONAL BLOCK DIAGRAM



ENOB = n_{R} -1-log₂(v)=16-1-1.85 \cong 13.15

Is this close to 16-bit performance?

A data clock output (DCO) for capturing data on the output is provided for signaling a new output bit.

The internal power-down feature supported via the SPI typically consumes less than 5 mW when disabled.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data test patterns.

The AD9467 is available in a Pb-free, 72-lead, LFCSP specified over the -40°C to +85°C industrial temperature range.

Test Setup Quite Sophisticated

From ADI AN-835



Figure 1. Typical Characterization Test Setup

Test Setup Quite Sophisticated

From ADI AN-835



Figure 2. Typical HSC-ADC-EVALC Evaluation Platform

Test Setup Quite Sophisticated

From ADI AN-835



Can we depend on this "13-bit" INL performance?

SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = -1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 1.							
Parameter ¹	Temp	Min	Тур	Max	Unit		
RESOLUTION		16			Bits		
ACCURACY							
No Missing Codes	Full		Guarantee	d			
Offset Error	Full	-200	0	+200	LSB		
Gain Error	Full	-3.9	-0.1	+2.6	%FSR		
Differential Nonlinearity (DNL) ²	Full	-0.9	±0.5	+15	LSB		
Integral Nonlinearity (INL) ²	Full	-12	±3.5	+12	LSB		
TEMPERATURE DRIFT				~	/		
Offset Error	Full		±0.023		%FSR/°C		
Gain Error	Full		±0.036		%FSR/°C		
ANALOG INPUTS							
Differential Input Voltage Range (Internal VREF = 1 V to 1.25 V)	Full	2	2.5	2.5	V p-p		
Common-Mode Voltage	25°C		2.15		V		
Differential Input Resistance	25°C		530		Ω		
Differential Input Capacitance	25°C		3.5		pF		
Full Power Bandwidth	25°C		900		MHz		
XVREF INPUT							
Input Voltage	Full	1		1.25	V		
Input Capacitance	Full		3		pF		
POWER SUPPLY							
AVDD1	Full	1.75	1.8	1.85	V		
AVDD2	Full	3.0	3.3	3.6	V		
AVDD3	Full	1.7	1.8	1.9	V		
DRVDD	Full	1.7	1.8	1.9	V		
AVDD1	Full		567	620	mA		
AVDD2	Full		55	61	mA		
AVDD3	Full		31	35	mA		
DRVDD	Full		40	43	mA		
Total Power Dissipation (Including Output Drivers)	Full		1.33	1.5	w		
Power-Down Dissipation	Full		4.4	90	mW		

¹ See the AN-835 Application Note, Understanding High Speed ADC Testing and Evaluation, for a complete set of definitions and how these tests were completed. ² Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.

ENOB = n_{R} -1- $\log_2(v)$ = 16-1-3.58 \approx 11.42

From INL viewpoint, performance is about 4.5 bits less than physical resolution but does have other attractive properties

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = -1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Parameter 1	Temp	Min	Тур Ма	c Unit
ANALOG INPUT FULL SCALE		2.5	2/2.5	V p-p
SIGNAL-TO-NOISE RATIO (SNR)				
f _{IN} = 5 MHz	25°C		74.7/76.4	dBFS
f _N = 97 MHz	25°C		74.5/76.1	dBFS
f _{IN} = 140 MHz	25°C		74.4/76.0	dBFS
f _{IN} = 170 MHz	25°C	73.7	74.3/75.8	dBFS
	Full	71.5		dBFS
fin = 210 MHz	25°C		74.0/75.5	dBFS
f _{IN} = 300 MHz	25°C		73.3/74.6	dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)				
f _N = 5 MHz	25°C		74.6/76.3	dBFS
f _N = 97 MHz	25°C		74.4/76.0	dBFS
f _N = 140 MHz	25°C		74.4/76.0	dBFS
f _N = 170 MHz	25°C	72.4	74.2/75.8	dBFS
	Full	71.0		dBFS
f _N = 210 MHz	25°C		73.9/75.4	dBFS
fn = 300 MHz	25°C		73.1/74.4	dBFS
EFFECTIVE NUMBER OF BITS (ENOB)				
fin = 5 MHz	25°C		12.1/12.4	Bits
f _N = 97 MHz	25°C		12.1/12.3	Bits
fin=140 MHz • Can be defined different ways	25°C		12.1/12.3	Bits
f _N = 170 MHz	25°C		12.0/12.3	Bits
 Only given as typical 	Full	11.5		Bits
f _N = 210 MHz	25°C		12.0/12.2	Bits
f _{IN} = 300 MHz	25°C		11.9/12.1	Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR) (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)				
f _{IN} = 5 MHz	25°C		98/97	dBFS
f _N = 97 MHz	25°C		95/93	dBFS
f _N = 140 MHz	25°C		94/95	dBFS
f _{IN} = 170 MHz	25°C	82	93/92	dBFS
	Full	82		dBFS
$f_{N} = 210 \text{ MHz}$	25°C		93/92	dBFS
f _N = 300 MHz	25°C		93/90	dBFS
SFDR (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)				
f _N = 5 MHz at -2 dB Full Scale	25°C		100/100	dBFS
f _N = 97 MHz at –2 dB Full Scale	25°C		97/97	dBFS
f _N = 140 MHz at-2 dB Full Scale	25°C		100/95	dBFS
f _{IN} = 170 MHz at -2 dB Full Scale	25°C		100/100	dBFS
f _N = 210 MHz at -2 dB Full Scale	25°C		93/93	dBFS
f _{IN} = 300 MHz at -2 dB Full Scale	25°C		90/90	dBFS
WORST OTHER (EXCLUDING SECOND AND THIRD HARMONIC DISTORTION)				
f _{IN} = 5 MHz	25°C		98/97	dBFS
f _N = 97 MHz	25°C		97/93	dBFS
f _{IN} = 140 MHz	25°C		97/95	dBFS
f _{IN} = 170 MHz	25°C	88	97/93	dBFS
	Full	82		dBFS
f _{IN} = 210 MHz	25°C		97/95	dBFS
fn = 300 MHz	25°C		97/95	dBES

Since the break-point INL is ideally 0, it is not related to either X_{LSB} or X_{REF} . As such, the magnitude of the break-point INL is independent of the resolution. It is thus difficult to naturally define the effective number of bits (ENOB) directly from the INL. However, since the gain (from input to interpreted output) of an ADC is ideally 1, the break-point INL is conveying about the same linearity information as the continuous-input INL. As such, the ENOB based upon the break-point INL is also defined by the same expression.

The ENOB based upon INL for both DACs and for ADCs is given by the expression

$$\mathsf{ENOB} = \mathsf{n}_{\mathsf{R}} - 1 - \mathsf{log}_2(\upsilon)$$

where n_R is the specified resolution and v is the INL in LSB at the n_R bit level.

Observe: the ENOB based upon the INL has been defined as the maximum deviation from the end-point fit line

The ENOB based upon INL for both DACs and for ADCs is given by the expression

$$\mathsf{ENOB} = \mathsf{n}_{\mathsf{R}} - 1 - \mathsf{log}_2(\upsilon)$$

where n_R is the specified resolution and v is the INL in LSB at the n_R bit level.

Observe: the ENOB based upon the INL has been defined as the maximum deviation from the end-point fit line

Question: With this definition, is it possible for a data converter to have an ENOB that is actually larger than n_R ? YES !

Question: What is the ENOB of any 1-bit ADC? ∞ !

Question: Is it easy to design a 4-bit ADC with an ENOB of 7 bits? YES !

Question: Is it easy to design a 14-bit ADC with an ENOB of 16 bits? No !

Question: Is ENOB (based on INL) a systematic metric?



Interpretation of ENOB definition for a DAC:

A DAC with n_{EFF} bits (ENOB) of resolution should have all outputs bounded by +/- $X_{LSBE}/2$ from the fit line so distance between fit line and upper/lower bounding lines determines the ENOB (X_{LSBE} is relative to n_{EFF} bits)

The ENOB based upon INL for both DACs and for ADCs is given by the expression

$$\mathsf{ENOB} = \mathsf{n}_{\mathsf{R}} - 1 - \mathsf{log}_2(\upsilon)$$

where n_R is the specified resolution and v is the resolution in LSB at the n_R bit level.

Observation: The ENOB was defined relative to a fit line and was not dependent upon the number of DAC levels or the number of break points in the ADC

Question: Then, why does n_R appear in the ENOB expression?

Question: Then, why does n_R appear in the ENOB expression?

ENOB = n_R -1-log₂(v)



Normalization was with respect to the LSB which is dependent upon n_R

Theorem: The INL ENOB is an inherent property of a data converter independent of the number of bits of resolution specified for a data converter

Proof: Assume a data converter has n_{RA} bits of resolution and an INL of v_A LSB and a converter with the same linearity was specified with n_{RB} bits of resolution and an INL of v_B LSB.

Since there are simply two representations of the same nonlinearity, the absolute INL will be the same for both representations. That is, $INL_A=INL_B$ (1)

Based upon the first specification, the INL can be expressed as

$$NL_{A} = v_{A} X_{LSBA}$$
(2)

But since it is assumed to have n_{RA} bits of resolution

$$\frac{X_{\text{LSBA}}}{X_{\text{REF}}} = 2^{-n_{\text{RA}}}$$
(3)

Proof (cont)

Thus we obtain the expression

$$INL_{A} = v_{A} 2^{-n_{RA}} X_{REF}$$
(4)

and the ENOB is given by

$$\mathsf{ENOB}_{\mathsf{A}} = \mathsf{n}_{\mathsf{R}\mathsf{A}} - 1 - \mathsf{log}_2(\upsilon_{\mathsf{A}}) \tag{5}$$

Substituting from (4) into (5) we obtain

$$\mathsf{ENOB}_{\mathsf{A}} = \mathsf{log}_2(\mathsf{X}_{\mathsf{REF}}) - 1 - \mathsf{log}_2(\mathsf{INL}_{\mathsf{A}}) \tag{6}$$

By a similar argument we obtain

$$\mathsf{ENOB}_{\mathsf{B}} = \mathsf{n}_{\mathsf{RB}} - 1 - \log_2(\upsilon_{\mathsf{B}}) \tag{7}$$

and

$$\mathsf{ENOB}_{\mathsf{B}} = \log_2(\mathsf{X}_{\mathsf{REF}}) - 1 - \log_2(\mathsf{INL}_{\mathsf{B}})$$
(8)

Now, since $INL_A = INL_B$, it follows that

Theorem: The INL-based ENOB can be equivalently expressed as

$$\mathsf{ENOB} = \mathsf{log}_2(\mathsf{X}_{\mathsf{REF}}) - \mathsf{log}_2(\mathsf{INL}_{\mathsf{REF}}) - 1$$

where INL_{REF} is the INL expressed relative to X_{REF} .

Proof: follows directly from proof of previous theorem

 $\mathsf{ENOB}=\mathsf{ENOB}_{\mathsf{A}}=\mathsf{log}_{2}(\mathsf{X}_{\mathsf{REF}})-1-\mathsf{log}_{2}(\mathsf{INL}_{\mathsf{A}})=\mathsf{log}_{2}(\mathsf{X}_{\mathsf{REF}})-1-\mathsf{log}_{2}(\mathsf{INL}_{\mathsf{REF}})$

To avoid possible misinterpretation, INL_{REF} defined below

$$INL_{REF} = \frac{INL_{V}}{V_{REF}}$$

where INL_{V} is the deviation in volts from the end-point fit line and $X_{\text{REF}}\text{=}V_{\text{REF}}$

Theorem: The INL-based ENOB can be equivalently expressed as

$$= \operatorname{NOB} = \operatorname{log}_2(X_{\operatorname{REF}}) - \operatorname{log}_2(\operatorname{INL}_{\operatorname{REF}}) - 1$$

where INL_{REF} is the INL expressed relative to X_{REF} .

Again, observe the INL-based ENOB does not depend upon the number of bits of resolution !

Recall previous question: can the INL-based ENOB on an n-bit ADC or DAC exceed n?

The answer was YES but in such a data converter it would probably be relatively easy to increase the number of bits of resolution while maintaining the ENOB, but applications would probably be limited

If the INL-based ENOB of a data converter exceeds n, it is probably over-designed

Designing a data converter of more than 1 bit that has a high number of bits of linearity (as measured by ENOB) is challenging

Performance Characterization of Data Converters

- Static characteristics
 - Resolution
 - Y− Least Significant Bit (LSB)
 - Offset and Gain Errors
 - Absolute Accuracy
 - Relative Accuracy
 - Integral Nonlinearity (INL)
 - Differential Nonlinearity (DNL)
 - Monotonicity (DAC)
- Missing Codes (ADC)
 - Quantization Noise
 - Low-f Spurious Free Dynamic Range (SFDR)
 - Low-f Total Harmonic Distortion (THD)
 - Effective Number of Bits (ENOB)
 - Power Dissipation

Differential Nonlinearity (DAC)

Nonideal DAC



DNL(k) is the actual increment from code (k-1) to code k minus the ideal increment normalized to X_{LSB}

$$DNL(k) = \frac{X_{OUT}(k) - X_{OUT}(k-1) - X_{LSB}}{X_{LSB}}$$

Differential Nonlinearity (DAC)

Nonideal DAC



Increment at code k is a signed quantity and will be negative if $X_{OUT}(k) < X_{OUT}(k-1)$

$$DNL(k) = \frac{X_{OUT}(k) - X_{OUT}(k-1) - X_{LSB}}{X_{LSB}}$$
$$DNL = \max_{1 \le k \le N-1} \left\{ |DNL(k)| \right\}$$
$$DNL = 0 \text{ for an ideal DAC}$$

Monotonicity (DAC)

Nonideal DAC



Monotone DAC

Non-monotone DAC

Definition:

```
A DAC is monotone if \mathcal{X}_{OUT}(k) > \mathcal{X}_{OUT}(k-1) for all k
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Theorem:

A DAC is monotone if DNL(k)> -1 for all k

Differential Nonlinearity (DAC)

Nonideal DAC



Theorem: The INL_k of a DAC (when corrected for gain error and offset) can be obtained from the DNL by the expression $INL_{k} = \sum_{i=1}^{k} DNL(i)$

Caution: Be careful about using this theorem to measure the INL since errors in DNL measurement (or simulation) can accumulate

Corollary: The DNL of a DAC (when corrected for gain error and offset) can be expressed as

 $DNL(k)=INL_{k}-INL_{k-1}$

Differential Nonlinearity (DAC)

Nonideal DAC



Theorem: If the INL of a DAC satisfies the relationship

$$NL < \frac{1}{2} X_{LSB}$$

then the DAC is monotone

Note: This is a necessary but not sufficient condition for monotonicity

Differential Nonlinearity (ADC)

Nonideal ADC



DNL(k) is the code width for code k – ideal code width normalized to X_{LSB} DNL(k)= $\frac{\chi_{T(k+1)} - \chi_{Tk} - \chi_{LSB}}{\chi_{LSB}}$

Differential Nonlinearity (ADC)

Nonideal ADC



 $DNL(k) = \frac{\mathcal{X}_{T(k+1)} - \mathcal{X}_{Tk} - \mathcal{X}_{LSB}}{\mathcal{X}_{LSB}}$ $DNL = \max_{2 \le k \le N-1} \{ |DNL(k)| \}$

DNL=0 for an ideal ADC

Note: In some nonideal ADCs, two or more break points could cause transitions to the same code C_k making the definition of DNL ambiguous

Monotonicity in an ADC



Definition: An ADC is monotone if the

 $\vec{X}_{OUT}(\mathcal{X}_k) \ge \vec{X}_{OUT}(\mathcal{X}_m)$ whenever $\mathcal{X}_k \ge \mathcal{X}_m$

Note: Have used \mathcal{X}_{Bk} instead of \mathcal{X}_{Tk} in figure on right since more than one transition point corresponds to a given code

Note: Some authors do not define monotonicity in an ADC.

Missing Codes (ADC)



No missing codes

One missing code

Definition: An ADC has no missing codes if there are N-1 transition points and a single LSB code increment occurs at each transition point. If these criteria are <u>not</u> satisfied, we say the ADC has missing code(s).

Note: With this definition, all codes can be present but we still say it has "missing codes"

Note: Some authors claim that missing codes in an ADC are the counterpart to nonmonotonicity in a DAC. This association is questionable.

Missing Codes (ADC)



Weird Things Can Happen



- Multiple outputs for given inputs
- All codes present but missing codes

Be careful on definition and measurement of linearity parameters to avoid having weird behavior convolute analysis, simulation or measurements

Most authors (including manufacturers) are sloppy with their definitions of data converter performance parameters and are not robust to some weird operation

LSB Definition

 X_{LSB} appears in many performance specifications but the definition of X_{LSB} is generally not given. This can cause modest inconsistencies in the definition of some performance specifications.

What is X_{LSB}?

LSB Definition

 X_{LSB} appears in many performance specifications but the definition of X_{LSB} is generally not given. This can cause modest inconsistencies in the definition of some performance specifications.

```
What is X<sub>LSB</sub>?
```

Conventional Wisdom X_{LSB}



 $(X_{LSB}$ determined by specified resolution and can not be measured)

Alternate LSB Definition

 X_{LSB} appears in many performance specifications but a distinction in X_{LSB} that differs from that obtained from specified values for X_{REF} and n_R is generally not given. This can cause modest inconsistencies in the definition of some performance specifications.

DAC

Alternate definitions of X_{LSB} where N is the measured number of DAC output levels

where N is the measured number of DAC output levels and $X_0(N-1)$ and $X_0(0)$ are last and first outputs respectively

useful when extreme values do not occur at minimum and maximum input codes

useful for determining worst-case resolution of a DAC

 $X_{LSB} = \frac{\underset{k}{\max} \{X_{0}(k)\} - \underset{k}{\min} \{X_{0}(k)\}}{N-1}$

 $X_{LSB} = \frac{X_0 (N-1) - X_0 (0)}{N_1 - 1}$

 $X_{LSB} = \frac{X_{REF}}{N}$

 $X_{LSB} = \max_{k} \{X_{0}(k) - X_{0}(k-1)\}$

ADC

Similar definitions can be made for X_{LSB} of an ADC based upon the breakpoints

Alternate LSB Definition

Is the concept of an LSB that is based upon measurements useful?

In many control applications, the largest gap between outputs of a DAC is often of interest and though that is ideally $V_{\rm LSB},$ it may differ significantly

ENOB based upon DNL

If it is assumed that an acceptable DNL for an n-bit data converter is $X_{LSB}/2$, then if the DNL is different from $X_{LSB}/2$, the effective number of bits essentially changes.

An ENOB based upon the DNL can be defined (homework problem)

ENOB relative to resolution

Summary of previous observations relating to ENOB (based upon INL) :

If an n-bit data converter has an INL of $\frac{1}{4}$ LSB, it is really performing from a linearity viewpoint at the n+1 bit level and if it has an INL of 1/8 LSB it is really performing at the n+2 bit level

Correspondingly, if it has a DNL of ¼ LSB, it is also performing from a differential linearity viewpoint at the n+1 bit level

The ENOB (based upon INL) of a data converter can exceed the number of bits of resolution of the data converter

Some applications benefit from an ENOB that exceeds the resolution of the data converter

- INL is a key parameter that is attempting to characterize the overall linearity of a DAC !
- INL is a key parameter that is attempting to characterize the overall linearity of an ADC !
- DNL is a key parameter that is attempts to characterize the local linearity of a DAC !
- DNL is a key parameter that is attempts to characterize the local linearity of an ADC !

Are INL and DNL effective at characterizing the linearity of a data converter?

Consider the following 4 transfer characteristics, all of which have the same INL







Although same INL, dramatic difference in performance particularly when inputs are sinusoidal-type excitations

INL also gives little indication of how performance degrades at higher frequencies Spectral Analysis often used as an alternative (and often more useful in many applications) linearity measure for data converters



Stay Safe and Stay Healthy !

End of Lecture 3